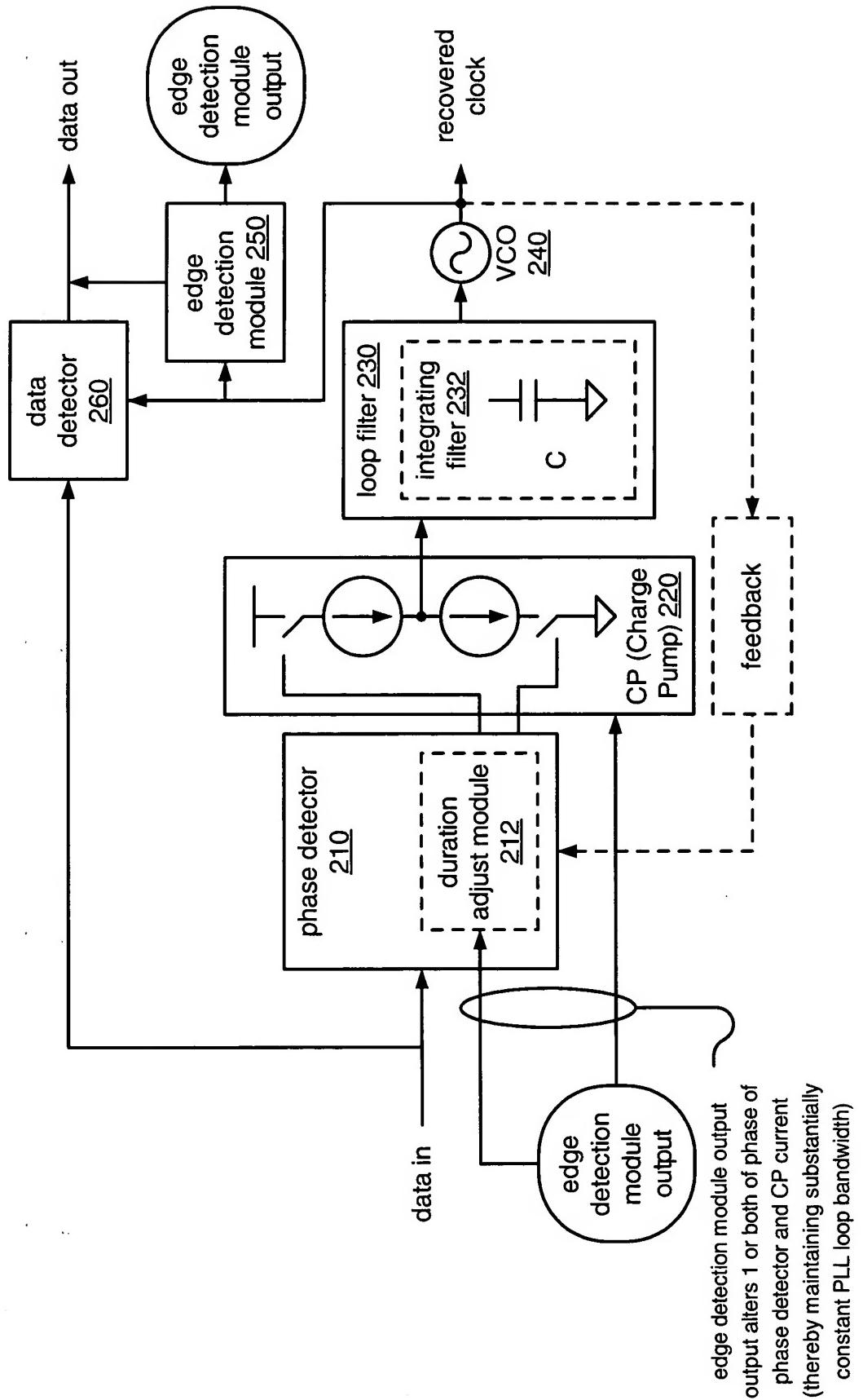
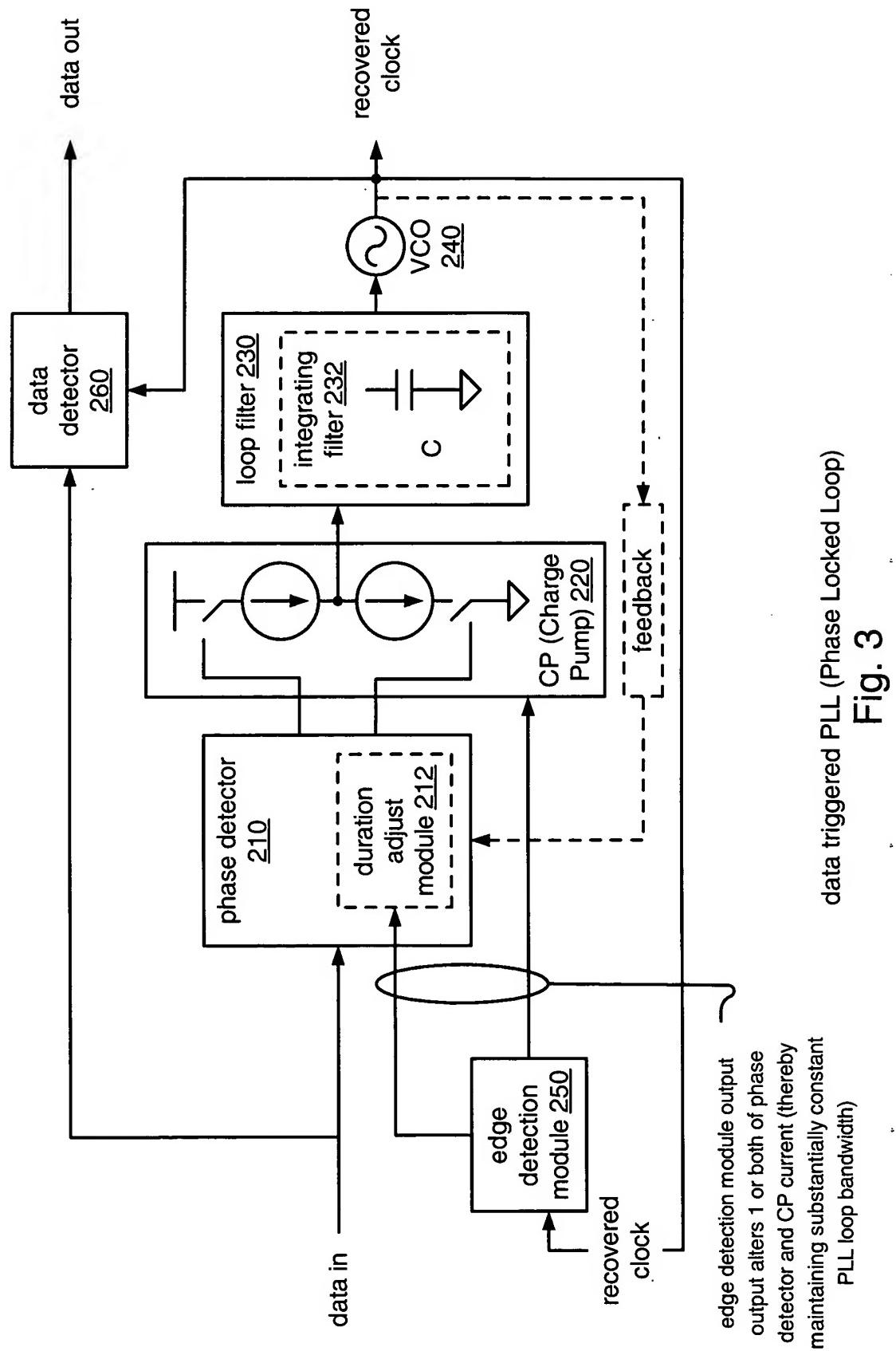


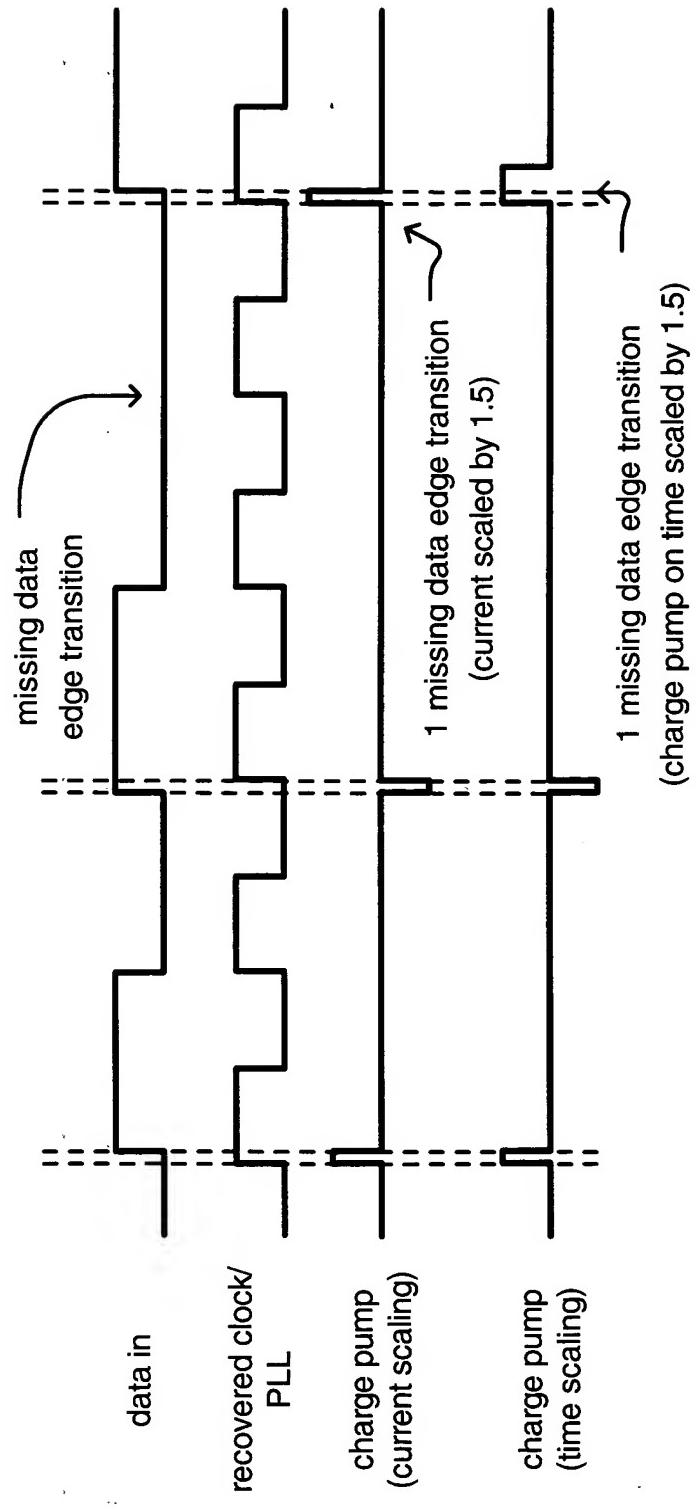
PLL (Phase Locked Loop)
Fig. 1
 (prior art)



data triggered PLL (Phase Locked Loop)

Fig. 2



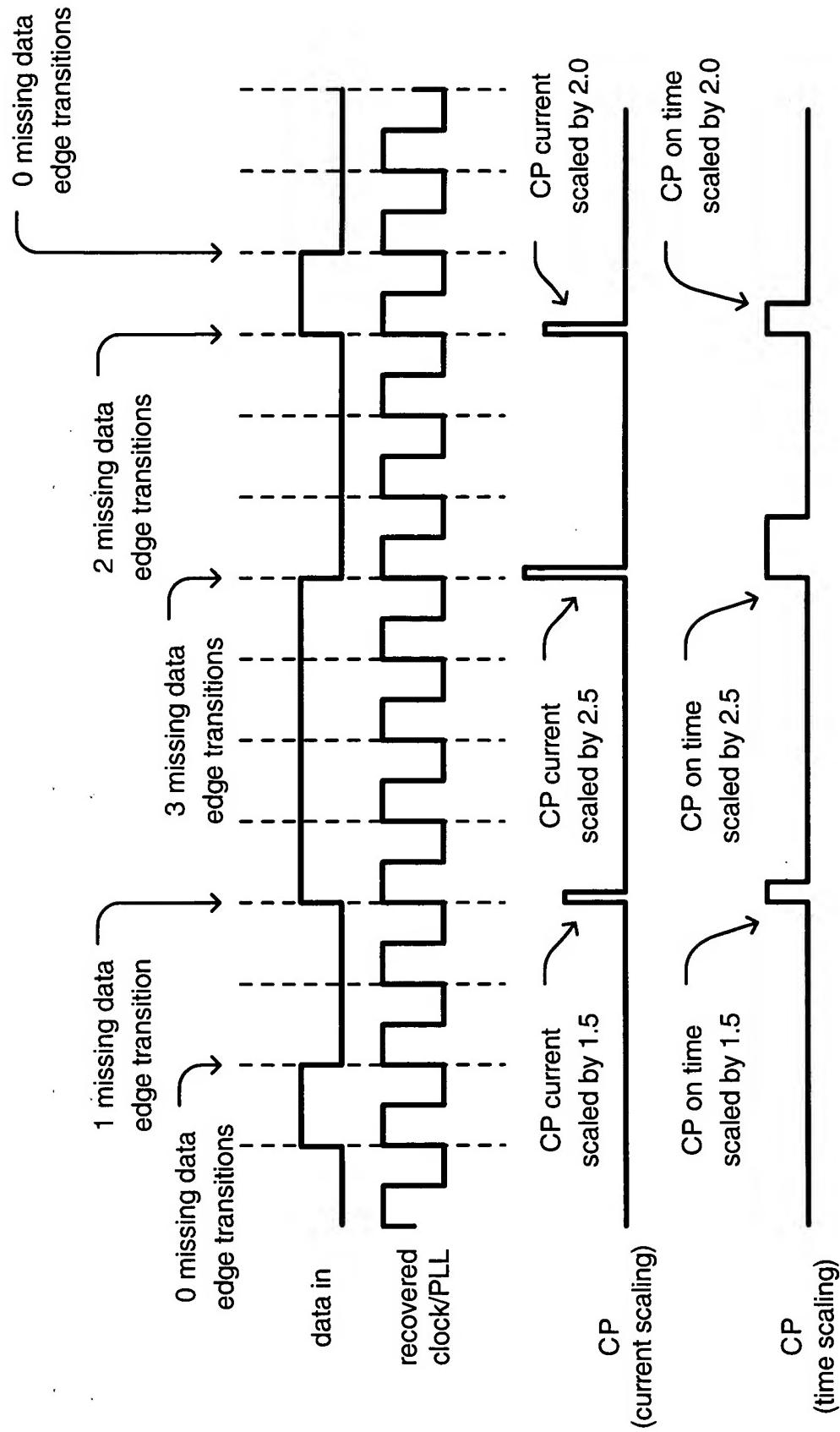


✓ may alternatively implement non-linear shift in PLL phase relative to data phase in absence of data edge transitions

# missing data edge transitions	phase error normalized to 1 on edges	sum
0		1
1	1/2	1.5
2	2/3	2.0
3	3/4	2.5
4	4/5	3.0
...

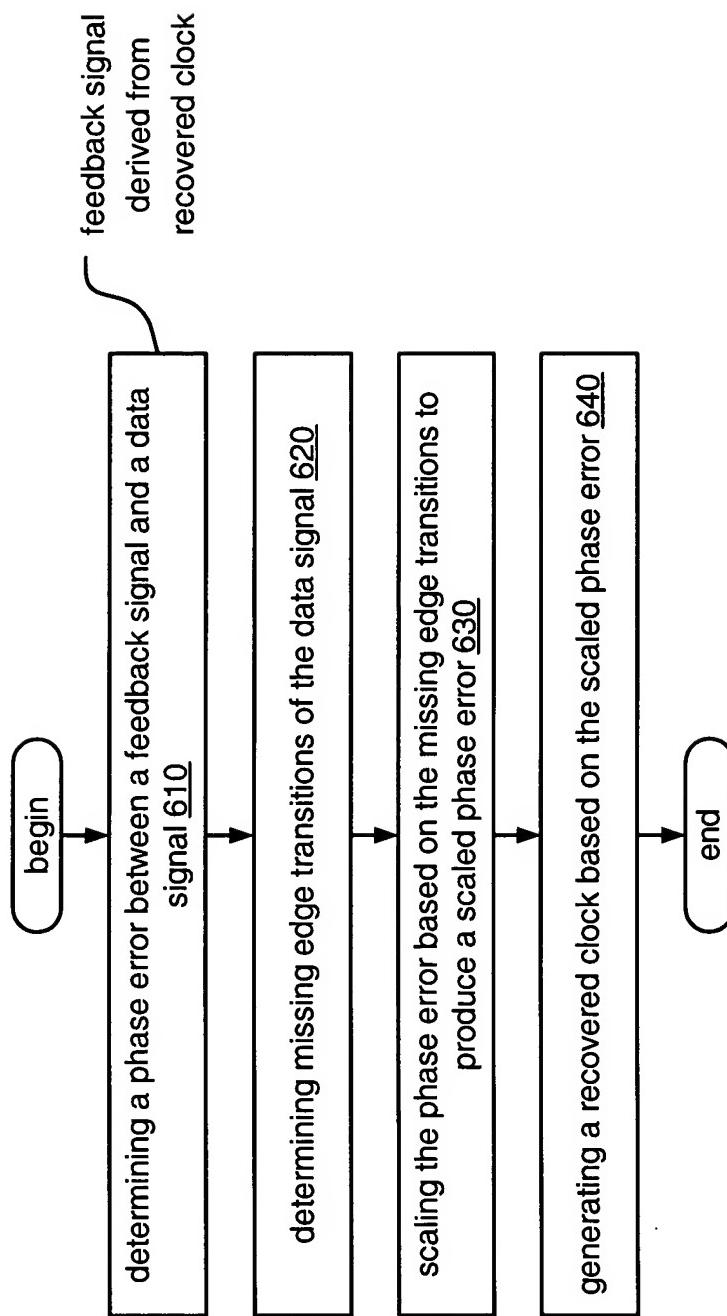
programmable CP current (or on time) that adapts to data edge transition density within data triggered PLL

Fig. 4



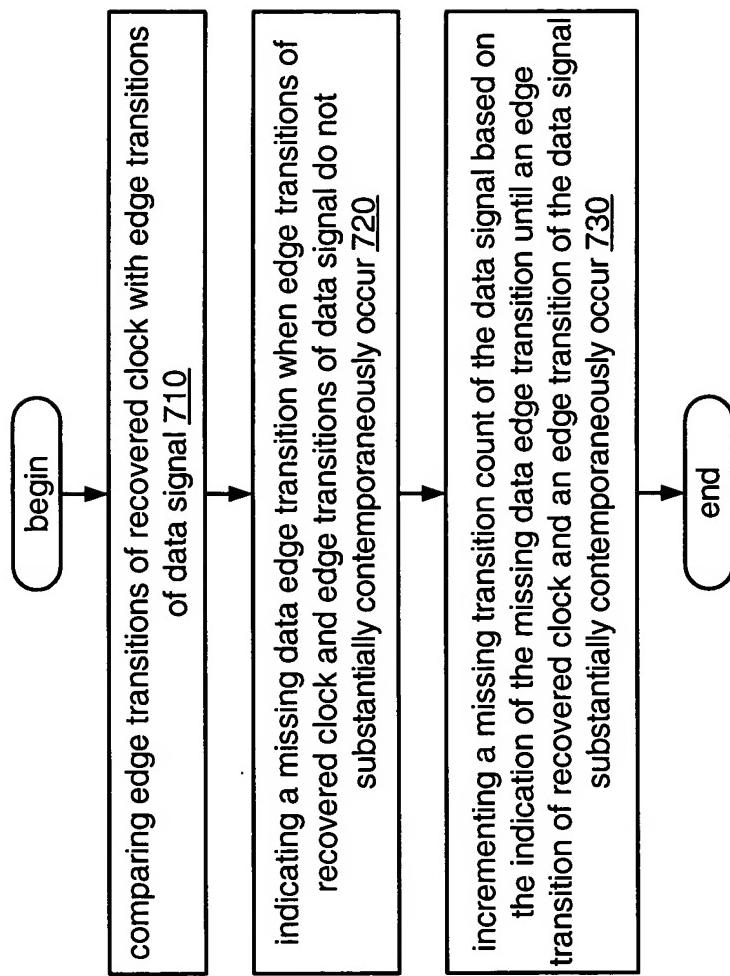
programmable CP current (or on time) that adapts to data edge transition density within data triggered PLL

Fig. 5



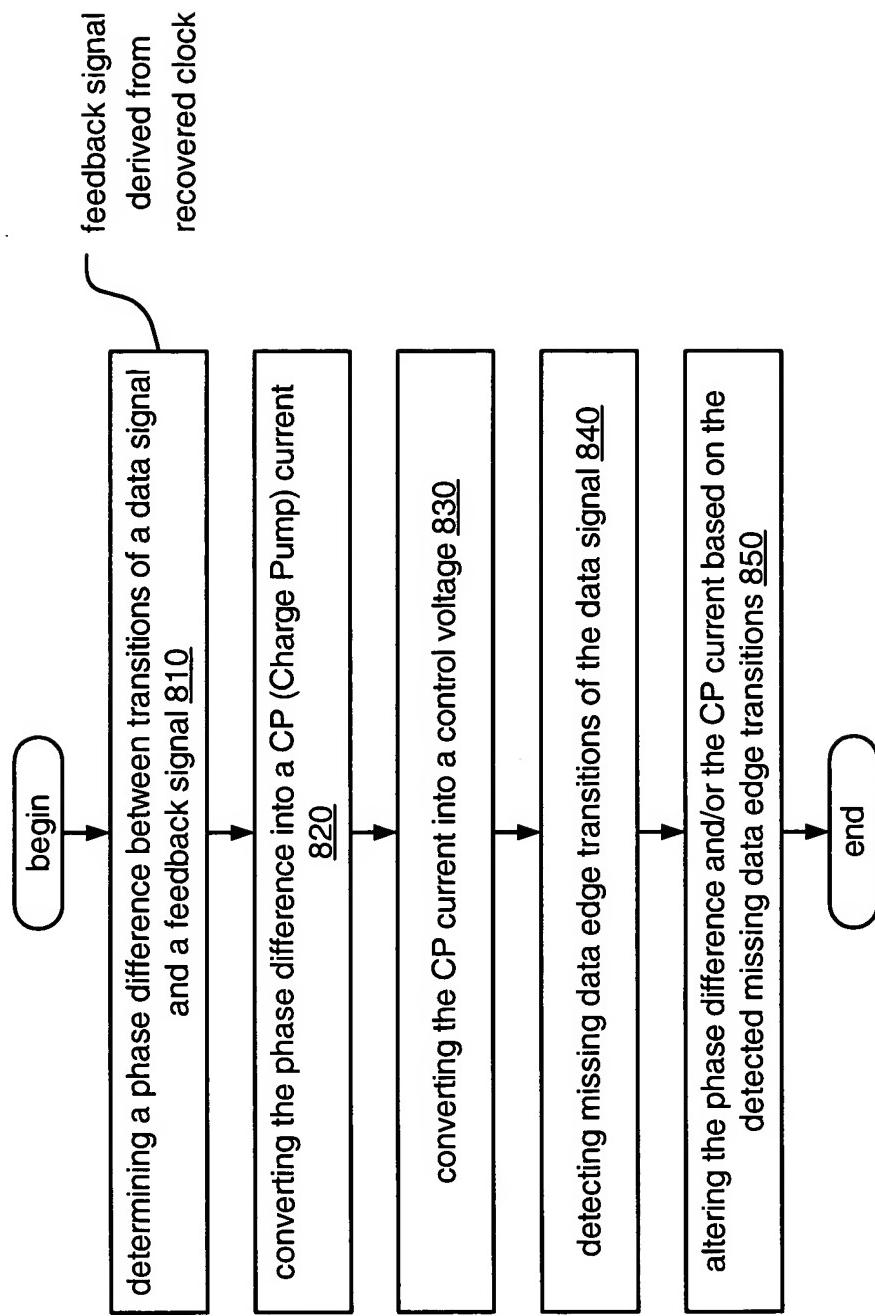
method for recovering clock from a data signal

Fig. 6



method for determining missing edge transitions of the data signal

Fig. 7



method for recovering clock from a data signal

Fig. 8